

# Matthew DeVuyst

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## Education

**Ph.D., Computer Engineering** 2011

University of California, San Diego

“Efficient Use of Execution Resources in Multi-Core Processor Architectures”

Advisor: Dean Tullsen

**M.S., Computer Science** 2006

University of California, San Diego

**B.A., Computer Science** 2003

Point Loma Nazarene University

## Professional Experience

**Research Assistant**, University of California, San Diego 2004 – 2009

Conducted computer architecture research to improve how legacy applications take advantage of modern multicore processors. Developed processor simulators and compilers (used C, C++, Python, assembly).

**Teaching Assistant**, University of California, San Diego 2003 – 2010

Supported instruction in computer science and engineering classes.

**Intern**, Teradata/NCR 2004

Added a security and authentication layer to database monitoring software (written in Java).

**Intern**, TrellisWare Technologies, Inc. 2003

Wrote a VHDL code obfuscator (in Perl) to protect company’s intellectual property.

**Intern**, Central Intelligence Agency 2001 – 2003

**Computer Technician**, Point Loma Nazarene University, IT Dept. 2000 – 2002

Serviced and repaired faculty and staff workstations, lab machines, and campus network.

## Selected Publications

*Execution Migration in a Heterogeneous-ISA Chip Multiprocessor*

Matthew DeVuyst, Ashish Venkat, Dean M. Tullsen.

*Proceedings of Seventeenth the International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)*, March 2012.

*Runtime Parallelization of Legacy Code on a Transactional Memory System*

Matthew DeVuyst, Dean M. Tullsen, Seon Wook Kim.

*Proceedings of the 6th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC)*, January 2011.

*Exploiting Unbalanced Thread Scheduling for Energy and Performance on a CMP of SMT Processors*

Matthew DeVuyst, Rakesh Kumar, Dean M. Tullsen.

*Proceedings of the IEEE International Parallel and Distributed Processing Symposium 2006 (IPDPS)*, April, 2006.

## Research

I've led research projects in the following areas:

**Thread scheduling:** We introduced novel scheduling algorithms for energy efficiency on multithreaded multiprocessors that result in an energy-delay product savings of 10%.

**Automatic Program Parallelization:** We proposed a mechanism to automatically parallelize legacy programs at runtime using a dynamic optimization framework and transactional memory resulting in a 35% performance improvement using two cores.

**Process Migration:** We proposed a new technique to rapidly migrate running programs on heterogeneous-ISA chip multiprocessors.

## Teaching

I love teaching and was a teaching assistant for the following courses at UCSD:

- *Introduction to Computer Architecture* 2010
- *Introduction to Computer Architecture Lab* 2006, 2009, 2010
- *Principles in Computer Architecture (grad class)* 2003, 2005, 2009
- *Computer Security* 2007, 2009

## Skills

Programming languages: **C** (expert), **C++** (proficient), **Python** (proficient), **Java** (prior experience), **Perl** (prior experience), **assembly** (prior experience)

Certifications: Microsoft Certified Systems Engineer, Cisco Certified Network Associate, CompTIA A+

## Software Projects

I have had the privilege of working on the following software projects:

- **GCC:** I added support for compiling for multiple targets to allow for easy process migration.
- **M5 Processor Simulator:** I added support for simulating ARM processors.
- **SMTSIM Processors Simulator:** I added a transactional memory system and integrated a power simulation model.